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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,071	11/19/2003	Darren L. Anand	BUR920030168US1	1070

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,071	ANAND ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to the Amendment filed 7/27/2007.

Claims 1-22 were previously rejected in the prior Office Action.

Claims 23-25 are new. Claims 1-25 are presently under examination and still pending in the Application.

Objection to the Claims for lack of paragraph indentations has been withdrawn in view of the amendment to the claims.

Response to Arguments

Applicant's arguments filed 7/27/2007, with respect to Claims 1-25, have been fully considered but they are not persuasive.

In reference to independent Claims 1, 7, 13 and 17, as currently amended, Applicant argues that the claimed invention now claims that the same register (Fail Map Register 11) used to capture the failed data is the same register that is used to also transfer the data to the tester, e.g., in a serial fashion. Applicant further argues that this is not the case in Nadeau-Dostie where the fail summary data must be transferred in a synchronous manner from a Failure Data Selector (element 178, Fig. 8 of Nadeau-Dostie) to a separate Transfer Register (180, Fig. 8 of Nadeau-Dostie).

In response to Applicant's argument, the Examiner notes that the above Applicant's arguments are not recited in the claims. Instead, the claims, as currently amended, recite that the "BIST generates a fail map data for capture by a diagnostic register device". Clearly, the Transfer Register of in the failure information 164, as

disclosed by Nadeau-Dostie, captures the diagnostic summary data associated with failures in the embedded memory 152 under test.

Assuming arguendo as alleged by the Applicant, that the Transfer Register 180, Fig. 8 of Nadeau-Dostie is a separate entity clocked synchronously with a slower transfer clock, the Examiner notes there is no recitation in the claims as to indicate that Applicant's diagnostic register device is a non separate entity operating non-synchronously at speed. Instead, the claimed invention recites "an external clock of the tester to read bit fail data out from said diagnostic register device to the tester", which clearly operates at slower speeds than the internal high speed multiplied clock. Still there is no recitation in the claims that the external clock is operates non-synchronously with respect to the internal clock.

In response to applicant's argument, it is noted that the features upon which applicant relies in his arguments are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 23-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 23-25 recite the newly added limitation "wherein new fail map data can be captured on every high speed multiplied clock cycle", which renders the claims indefinite, because the expression "can be" implies that there may be instances where data is not always captured. Therefore, the expression does not constitute a positive limitation in any patentable sense.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7, 8, 13, 17-19 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. (US 20050047229) US Application 10/690594, filed: October 23, 2003.

Regarding independent Claims 1, 7, 13, 17, Nadeau-Dostie discloses a method and a circuit for collecting memory failure information 164 on-chip and unloading the information in real time while performing at-speed test of an embedded memory 152 using a memory test controller 150, Fig. 7, comprising:

Using a high speed (system clock) for testing each memory location of the column or row of a memory under test (152) according to a memory test algorithm under the control of the system clock, and transferring the failure summary via a circuit serial output under the control of an (ExtClock) tester clock concurrently with testing of the next column or row in sequence, see Summary of the Invention. The system clock is multiple and synchronous with the ExtClock, as shown in Fig. 9,which is a detailed timing diagram, showing the (system clock) used to perform the memory test, and the ExtClock, which generates the synchronization pulses (SyncPulse) to synchronize the transfer of the failure summary to the tester.

During read operations, the memory data output is compared (step 30) against an expected value. If the data is different, a failure has been detected and is classified (step 34) according to predetermined failure types, thus pausing the testing at the end of a column or row test.

Using the ExtClock of the tester to read bit fail data from the failure summary block 164 out to the tester. When the test of a column or row has been completed, column or row failure summary is generated (step 47), loaded into a transfer register, and scheduled to be transferred off-chip (step 48) under the control of the ExtClock.

The failure summary is transferred serially. However, the summary may also be transferred in parallel. After completing a test phase, when the last column (or row) has been tested (step 50), a phase failure summary may be generated and possibly encoded (step 52) and transferred off-chip (step 54).

Resuming the BIST testing with the high speed (system clock) by beginning the test phase (step 20), and by next performing read and write operations (step 28) according to a memory test algorithm under control of the system clock.

Regarding Claim 2, 8, Nadeau-Dostie discloses a method and a circuit for collecting memory failure information 164 on-chip and unloading the information in real time while performing at-speed test of an embedded memory 152, such as a Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) bitmaps of interest and potential failure causes, as shown in Fig. 2.

Regarding Claims 18, 19, Nadeau-Dostie discloses Failure data selector 178 loads summary data to be output from the circuit into a transfer register 180 and may also encode data according to a predetermined encoding scheme. Alternatively, data could be encoded prior to delivery to selector 178. The data loaded into the transfer register depends on the specific failure summary combination, which was designed for the circuit, the access mode and phase of a test. The transfer register operates under control of the Clock signal and a small finite state machine (FSM) 182. The transfer register has a serial input and a serial output and a clock input which receives the Clock signal. FSM 42 includes a counter 184, which counts the number of bits, which have been loaded/unloaded into/from the transfer register.

Regarding Claims 23-25, new fail map data are captured in the failure summary generator block 164, using a high speed (system clock), Figs. 8 and 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6, 9-12, 14-16 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. (US 20050047229) in view of Hirabayashi (US Patent No. 6,978,402).

Regarding Claims 3, 4, 6, 9, 10, 12, 14, 16, 20, 22, Nadeau-Dostie does not explicitly disclose, "an on-chip clock multiplier to multiply the external clock to generate a high speed multiplied clock and a multiplexer to pass either the tester clock or the high speed multiplied clock".

However, in analogous art, Hirabayashi (US Patent No. 6,978,402) discloses a clock generator 11, Figs. 3-6, which receives an external clock signal CK and includes an oscillator 111, which generates a high-frequency clock signal, and a multiplexer 113, which selects, as an internal clock signal CK_int, the external clock signal CK_ext or the high-frequency clock signal. In a normal mode, the multiplexer 113 selects the external

clock signal CK_ext as the internal clock signal CK_int. In a high-speed test mode, the multiplexer 113 selects the high-frequency clock signal generated by the oscillator 111 as the internal clock signal CK_int.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the clock generator as taught by Hirabayashi in the embedded memory test controller of Nadeau-Dostie for the purpose of carrying out high-speed testing of embedded memories using built-in self test (BIST) circuit, thus avoiding the use of expensive High-speed testers.

Regarding Claims 5, 11, 15, 21, Nadeau-Dostie discloses a failure summary generator 164, which receives various inputs from comparators block 162 at a system clock rate, but transfers failure summary to a tester at a tester clock rate, which is usually significantly lower than the system clock rate, Figs. 7 and 8. After completing a test phase, when the last column (or row) has been tested (step 50), a phase failure summary may be generated and possibly encoded (step 52) and transferred off-chip (step 54), Fig. 3.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection (under 35 U.S.C. 112, second paragraph) presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

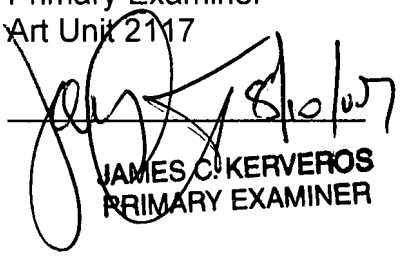
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2117



Date: 10 August 2007
Office Action: Final Rejection

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